REMARKS

The claims are claims 1, 4, 5, 13, 16, 17 and 25.

The application has been further amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner.

Claims 1, 4, 5, 13, 16, 17 and 25 have been amended. Claims 2, 3, 6 to 12, 14, 15, 18 to 24, 26 and 27 are canceled. Claims 1, 13 and 25 are amended to recite fixed length information blocks as disclosed in the application at page 21, line 14 to page 26, line 6 which describe an example 10-bit format. Claims 4 and 16 are amended to recite the storing comparison data and comparing this to emulation data and to include further detail of the compression map as described in the application at page 13, line 7 to page 33, line 2 and illustrated in Figure 12. Claim 16 is further amended to depend upon independent claim 13 rather than canceled claim 15. Claims 5 and 17 are amended to recite the timing bits as described in the application at page 23, line 7 to page 24, line 6 and illustrated in Figures 3 and 4.

Claims 1, 5, 13, 17 and 25 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards et al U.S. Patent No. 6,918,065 (Edwards '065) and Edwards et al U.S. Patent No. 6,530,047 (Edwards '047).

Claims 1, 13 and 25 recite subject matter not made obvious by the combination of Edwards '065 and Edwards '047. Claims 1, 13 and 25 recite that the information blocks had a "fixed length." The OFFICE ACTION cites Edwards '065 Figure 7 and Tables 1 to 3 as making obvious the recited information blocks. However, the trace message fields of Table 1 include a variable length (1, 2, or 4 bytes) program counter field. The trace message fields of Tables 2 and 3 include a variable length (0 or 1 bytes) timestamp field, a

variable length (0 or 1 bytes) ASID and a variable length (1, 2, or 4 bytes) program counter field. To the extent that Edwards '065 discloses the differing the relative proportions of emulation control information and emulation data in other blocks of the sequence, this is achieved by variable length information blocks. This is contrary to the "fixed length" recited in claims 1, 13 and 25. Accordingly, claims 1, 13 and 25 are allowable over the combination of Edwards '065 and Edwards '047.

Claims 5 and 17 recite subject matter not made obvious by Edwards '065 and Edwards '047. Claims 5 and 17 recite that data in one information block "includes bits indicating whether the data processor performed data processing operations during a corresponding clock cycle." The OFFICE ACTION cites the timestamp field of Table 1 as making obvious this subject matter. Edwards '065 states at column 12, lines 31 to 34:

> "Timestamp **708** may be an optional field if circuit **103** is configured to include timestamp information within trace messages. Timestamp **708** may be, for example, a value which specifies a number of timer increments since a last reference trace message was generated (reference trace messages will be described in more detail below)."

This "value which specifies a number of timer increments" clearly differs from the recited indication "whether the data processor performed data processing operations during a corresponding clock cycle." Accordingly, claims 5 and 17 are allowable over the combination of Edwards '065 and Edwards '047.

Claims 4 and 16 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards et al U.S. Patent No. 6,918,065 (Edwards '065), Edwards U.S. Patent No. 6,530,047 (Edwards '047) and Riley U.S. Patent No. 5,832,490.

Claims 4 and 16 recite subject matter not made obvious by the combination of Edwards '065, Edwards '047 and Riley. Claim 4

recites "storing comparison data; comparing respective sections of emulation data with the stored comparison data" and "compression map indicative of whether the sections of the emulation data match the stored comparison data." Claim 16 likewise recites "a comparison data register storing comparison data; a comparitor connected to said comparison data register and receiving emulation data generating an indication of a match between corresponding sections of said comparison data and said emulation data" and "a compression map indicative of whether the sections of the emulation data match the stored comparison data." The OFFICE ACTION cites Riley at Figure 2 and column 4, lines 20 to 50 as making obvious this subject matter. Riley states at column 4, lines 31 to 33 (within the section cited in the OFFICE ACTION):

> "The bitfield header (also referred to herein as a 'map') comprises an array of 0's and 1's which indicate which of the data samples in datafield 210 are compressed or uncompressed."

The Applicant respectfully submits that this teaching of Riley is clearly a different indication for a different purpose than that recited in claims 4 and 17. Accordingly, claims 4 and 17 are allowable over the combination of Edwards '065, Edwards '047 and Riley.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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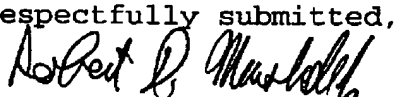
Respectfully submitted,



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